Curriculum Vitae

dr. ir. Hans Vandierendonck

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Contact Information

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Employment history

Aug '17–present	**Senior Lecturer**. School of Electronics, Electrical Engineering and Computer Science, Queen's University Belfast
Apr '12–Aug '17	**Lecturer**. School of Electronics, Electrical Engineering and Computer Science, Queen's University Belfast
Apr '13–Mar '15	**EC Marie Curie Fellow**. School of Electronics, Electrical Engineering and Computer Science, Queen's University Belfast
Oct '04–Mar '12	**Fellow of the Research Society Flanders (FWO)**. Faculty of Engineering and Architecture, Ghent University
Feb '04–Sep '04	**Postdoctoral Research Fellow**. Faculty of Engineering and Architecture, Ghent University

Education

1999 – 2004	PhD, Computer Engineering, Ghent University Belgium
1994 – 1999	MEng, Computer Engineering (Burgerlijk ingenieur in de computerwetenschappen), Ghent University, Belgium

Research Interests

System software: parallel computing, parallel programming languages, compilation, runtime systems, operating systems, large-scale data analytics.
Computer architecture: many-core architectures, memory hierarchy organisation, prediction techniques.
Modelling and evaluation of computing systems: performance; energy; profiling, instrumentation, simulation and modelling.

Other Appointments and Affiliations

- Member of the EPSRC College of Peer Reviewers (2013–present).
- Association for Computing Machinery (ACM), Senior Member (2013–present), Member (2001–2013).
- Institute of Electrical and Electronics Engineers (IEEE), Senior Member (2012–present), Member (1998–2012).
- Higher Education Academy, Fellow (2014–present).
- EU Network-of-Excellence "High-Performance and Embedded Architecture and Compilation" (HiPEAC). Member.

Honours and Awards

2015	Second place in ACM Student Research Competition for PhD student Ahmad Hassan
2004	Finalist 1st Journal of Instruction-Level Parallellism Championship Branch Prediction competition
2004	IBM Belgium Prize in Informatics awarded by the Research Foundation Flanders (FWO) – PhD thesis
2000	IBM Belgium Prize in Informatics awarded by the Research Foundation Flanders (FWO) – MEng thesis
2000	Jozef Plateau Prize awarded by the Alumni Engineers Ghent University (AIG) – MEng thesis

Refereed Publications

Published 2 invited book chapters, 25 A*/A refereed journal contributions and 63 refereed conference and workshop contributions.

Citation Metrics (Google Scholar)

Citations: 1375, h-index: 19, i-10 index: 36

Research Grants

Total amount of research awards as PI or CoI, including partner grant shares:	£22,305,140
Total amount of research awards as PI or CoI (ownership):	£1,414,699
QUB share of research awards lead as PI:	£735,122

Summary funding highlights: EC Marie Curie Fellowship, EPSRC First Grant (PI), EPSRC (Co-I on 4 projects), EC FP7 (PI), EC H2020 (Co-I on 3 projects).

1. **OPRECOMP: Open Transprecision Computing.** Sponsor: EC Horizon 2020. Role: Co-I. Grant amount: £486,639.00 Dates of activity: 01/2017–12/2021.
2. **UniServer: A Universal Micro-Server Ecosystem by Exceeding the Energy and Performance Scaling Boundaries.** Sponsor: EC Horizon 2020. Role: Co-I. Grant amount: £667,548.00. Dates of activity: 01/2016–12/2018.
3. **Versatile Integrated Accelerator-Based Heterogeneous Data Centres (VINEYARD).** Sponsor: EC Horizon 2020. Role: Co-I. Grant amount: £457,672.00. Dates of activity: 01/2016–12/2018.
4. **Scale-free, energy-aware and resilient adaptation of CSE applications to mega-core systems (SERT).** Sponsor: Engineering and Physical Sciences Research Council. Role: Co-I. Grant amount: £694,909.00. Dates of activity: 04/2015–03/2018.
5. **Hybrid static/dynamic scheduling for task dataflow parallel programs.** Sponsor: Engineering and Physical Sciences Research Council. Role: PI. Grant amount: £96,235.00. Dates of activity: 12/2014–02/2017.
6. **HPDCJ: Heterogeneous parallel and distributed computing with Java.** Sponsor: Engineering and Physical Sciences Research Council. Role: Co-I. Grant amount: £221,592.00. Dates of activity: 10/2014–09/2017.
7. **DIVIDEND: Distributed heterogeneous vertically integrated energy efficient data centres.** Sponsor: Engineering and Physical Sciences Research Council. Role: Co-I. Grant amount: £140,710.00. Dates of activity: 10/2014–09/2017.

8. **ASAP: An adaptive, highly scalable analytics platform.** Sponsor: EC Framework Programme 7. Role: PI. Grant amount: £346,701.00. Dates of activity: 01/2014–12/2016.
9. **UK-USA HPC Travel Grant (SC13).** Sponsor: Engineering and Physical Sciences Research Council. Role: PI. Grant amount: £2,500.00. Dates of activity: 10/2013–09/2014.
10. **Software management of hybrid DRAM/NVRAM memory systems (NovoSoft).** Sponsor: EC–Framework Programme 7, Marie Curie Intra-European Fellowship. Role: PI. Grant amount: £247,388.00. Dates of activity: 03/2013–02/2015.
11. **PhD Studentship: Characterising and optimising in-memory database systems for emerging memory technologies.** Sponsor: SAP UK Ltd. Role: PI. Grant amount: £34,298.00. Dates of activity: 03/2013–02/2016.
12. **Faculty Startup Grant.** Sponsor: Queen's Universtiy Belfast. Role: PI. Grant amount: £8,000. Dates of activity: 04/2012–present.
13. **Variability-aware program relocation (VAPOR).** Sponsor: Research Foundation Flanders. Role: Co-I (while at Ghent University, Belgium). Grant amount: €267,200.

Research Group

I am supervisor and line manager for 5 post-doctoral research fellows and 2 pre-doctoral research assistants. I am moreover primary supervisor of 2 PhD students and secondary (co-) supervisor for 2 PhD students.

PhD Student Supervision

Primary Supervisor

1. **Jiawen Sun**. EEECS, Queen's University Belfast. Co-supervised with Dimitrios S. Nikolopoulos. Subject: Efficient graph analytics on large-scale shared memory machines.
2. **Mahwish Arif**. EEECS, Queen's University Belfast. Co-supervised with Dimitrios S. Nikolopoulos and Bronis de Supinski. Subject: Measuring and Improving Performance Portability.
3. **Ahmad Hassan**. EEECS, Queen's University Belfast. Sponsored by SAP UK Ltd. Co-supervised with Dimitrios S. Nikolopoulos. Thesis title: Characterising and optimising in-memory database systems for emerging memory technologies. Graduated 2016.
4. **Sean Rul**, Ghent University, Belgium. Co-supervised with Koen De Bosschere. Thesis title: Profile-Driven Discovery of Parallelism for Multi-Core Processors. Graduated 2010.

Co-Supervisor

1. **Charalambos Chalios**. EEECS, Queen's University Belfast. Co-supervised with Dimitrios S. Nikolopoulos. Thesis title: Runtime systems for significance-based computing. Submitted dissertation.
2. **Konstantin Bakanov**. EEECS, Queen's University Belfast. Co-supervised with Ivor Spence. Research theme: streaming computations.

Service

Conference Committee Activities

I have served/am serving on the programme committees of several leading conferences (IPDPS '08, ISCA '10 (external programme committee), Supercomputing '14, CCGrid '14–'16, Euro-Par '15, '16, ICPP '17), conferences (SAAHPC '09–'11, DATE '07–'10, ARCS '12, '14–'17, ICPADS '16) and workshops (GPGPU '09, IFMT '09, MULTIPROG '16, '17, MEDAL '16, IWMSE '16, COSMIC '17). I regularly review for leading conferences (IPDPS, IISWC, ICS, DAC, Euro-Par) and journals in the field (ACM TACO, IEEE TC, IEEE TPDS, IEEE TSE, IEEE Micro, ACM TOPLAS, ACM ToDAES, Wiley CCPE, Elsevier JPDC, Elsevier Parallel Computing, Elsevier JSA, Elsevier Sustainable Computing).

I co-chair Track 9 on Multi-Core and Many-Core Parallelism at Euro-Par '17. I am Finance Chair for IEEE CLUSTER 2018. I was a member of the organizing comittee of the HiPEAC conference, 2009 (publicity chair) the International Symposium on Computer Architecture, 2010 (publicity chair) and the Symposium on High-Performance Computer Architecture, 2016 (student travel grant chair).

PhD and Master Thesis Examination

1. Member of the jury for the Master's thesis of Igor Loiselle and Thibault Delavallée (Université catholique de Louvain), 2006–2007, "Etude de la parallélisation des accès mémoire dans les processeurs superscalaires" (Study of the Parallelization of Memory Accesses in Superscalar Processors), Ingénieur civil Electromécanicien, mécatronique.
2. Member of the PhD jury of Imran Quadri, "MARTE based model driven design methodology for targeting dynamically reconfigurable FPGA based SoCs." for the degree of Doctor of Philosophy in computer science at the École Doctorale Sciences pour l'Ingénieur. Promotor: Prof. Jean-Luc Dekeyser, Université des Sciences et Technologies de Lille, France, 2010.
3. Member of the PhD jury of Sean Rul, "Profile-Driven Discovery of Parallelism for Multi-Core Processors." for the degree of Doctor in Engineering - Computer Science. Promotors Prof. Koen De Bosschere and Hans Vandierendonck, Ghent University, Ghent, Belgium, 2010.
4. Member of the PhD jury of Bertrand Rousseau, "Evaluations of Hardware Platforms, Methods and Tools for Low-Volume Software-Defined Signal Processing Applications" for the Degree of "Docteur en Sciences de l'Ingénieur". Promotor: Prof. Jean-Didier Legat, Université catholique de Louvain, Belgium. 2011.
5. External examiner for the Master's thesis of Olav Fagerlund, Promotor: Prof. Lasse Natvig, Department of Computer and Information Science, Norwegian University of Science and Technology (NTNU). September 2010. Title: "Multi-core programming with OpenCL: performance and portability."
6. Member of the comité d'accompagnement for the PhD of Igor Loiselle (Université catholique de Louvain), September 2007–current, "Mapping of parallel algorithms on a tiled multicore architecture".
7. Member of the commité d'accompagnement for the PhD of Thibault Delavallée (Université catholique de Louvain), September 2007–current, "Optimization and parallelization of memory instructions in tiled multicore architectures".
8. External examinar of the PhD dissertation of Juan Manuel Cebriàn González. "Efficient Power and Thermal Management using Fine-grain Architectural Approaches in Multicores." Advisors: Prof. Juan Luis Aragón and Prof. Stefanos Kaxiras, Computer Engineering Departement, University of Murcia, Spain, 2011.
9. Member of the PhD committee of Michail Alvanos. "Optimization techniques for fine-grained communication in PGAS environments". Advisors: Prof. Xavi Martorell, Prof. José Nelson Amaral and Prof. Montse Farreras. Universitat Polytècnica de Catalunya (UPC), Spain, 2013.
10. External examinar Barghava Rajaram. "Efficient, Scalable, and Fair Read-Modify-Writes" Advisor: dr. Vijay Nagajaran, School of Informatics, University of Edinburgh, 2014.
11. Internal examinar (anonymised as student failed viva), School of EEECS, Queen's University Belfast, 2015.
12. Member of the PhD committee of Giorgis Georgakoudis. "Scheduling and Performance Characterization on Heterogeneous Computing Systems". Advisor: Prof. Spyros Lalis, Prof. Dimitrios S. Nikolopoulos and Prof. Christos Antonopoulos, University of Thessaly, Greece, 2016.
13. External examinar Andras Chatzistergiou. "Programming language support for historical and persistent data-structures in non-volatile memories" Advisor: Prof. Stratis Viglas, School of Informatics, University of Edinburgh, 2016.

Complete List of Publications

(A1) Articles Included in the Science Citation Index

1. Hans Vandierendonck and Koen De Bosschere. **Highly Accurate and Efficient Evaluation of Randomising Set Index Functions**. Journal of Systems Architecture, 48(13–15):429–452, May 2003.

Impact factor in 2002: 0,210.

2. Lieven Eeckhout, Hans Vandierendonck and Koen De Bosschere. **Designing Computer Architecture Research Workloads**. IEEE Computer, 36(2):65–71, February 2003.
   Impact factor in 2010: 2.205, 1st quartile.
3. Hans Vandierendonck and Koen De Bosschere. **Randomized Caches for Power-Efficiency**. IEICE Transactions on Electronics, E86-C(10):2137-2144, October, 2003.
   Impact factor in 2002: 0,336.
4. Bjorn De Sutter, Hans Vandierendonck, Bruno De Bus and Koen De Bosschere. **On the Side-Effects of Code Abstraction**. ACM SIGPLAN Notices, 38(7):243-253, July 2003.
   Impact factor in 2002: 0,190.
5. Hans Vandierendonck and Koen De Bosschere. **On Generating Set Index Functions for Randomised Caches**. Computer Journal, 47(2):245-258, February 2004.
   Impact factor in 2002: 0,361.
6. Hans Vandierendonck and Koen De Bosschere. **XOR-Based Hash Functions**. IEEE Transactions on Computers, 54(7):800-812, July 2005.
   Impact factor in 2010: 1.822, 1st quartile.
7. Veerle Desmet, Hans Vandierendonck and Koen De Bosschere. **Clustered Indexing for Branch Predictors**. Microprocessors and Microsystems, 31(3):168–177, March 2007.
8. Hans Vandierendonck, Veerle Desmet and Koen De Bosschere. **Behavior-Based Branch Prediction by Dynamically Clustering Branch Instructions**. Journal of Information Science and Engineering, 24(3):919–931, 2008.
9. Hans Vandierendonck and André Seznec. **Speculative Return Address Stack Management Revisited**. ACM Transactions on Architecture and Code Optimization, 5(3), 2008.
10. Hans Vandierendonck, Sean Rul and Koen De Bosschere. **Accelerating Multiple Sequence Alignment with the Cell BE Processor**. The Computer Journal. pp. 814–826, 2010.
11. Sean Rul, Hans Vandierendonck and Koen De Bosschere. **A Profile-Based Tool for Finding Pipeline Parallelism in Sequential Programs**. Parallel Computing, 36(9):531–551, 2010.
    Impact factor 1.125, 1st quartile.
12. Hans Vandierendonck and Tom Mens. **Averting the Next Software Crisis**. IEEE Computer, 44(4):88–90, April 2011.
    Impact factor 2.205, 1st quartile.
13. Hans Vandierendonck and André Seznec. **Managing SMT Resource Usage through Speculative InstructionWindow Weighting**. ACM Transactions on Architecture and Code Optimization. Accepted for publication, 2011.
14. Hans Vandierendonck and Tom Mens. **Techniques and Tools for Parallelizing Software**. IEEE Software, 29(2):22–25, February 2012.
15. Hans Vandierendonck, George Tzenakis, Dimitrios S. Nikolopoulos. **Analysis of Dependence Tracking Algorithms for Task Dataflow Execution**. ACM Transactions on Architecture and Code Optimization, 10(4):61, 24 pages, 2013.
16. Dimitrios S. Nikolopoulos, Hans Vandierendonck, Nikos Bellas, Christos D. Antonopoulos, Spyros Lalis, George Karakonstantis, Andres Burg, Uwe Naumann. **Energy-Efficiency through Significance-Based Computing**. IEEE Computer, 47(7):82–85, 2014.
17. Philipp Gschwandter, Charalambos Chalios, Dimitrios S. Nikolopoulos, Hans Vandierendonck and Thomas Fahringer. **On the potential of significance-driven execution for energy-aware HPC**. Computer Science – Research and Development. 30(2):1865–2034, 2015.
18. Vassilis Vassiliadis, Charalambos Chalios, Konstantinos Parysis, Christos D. Antonopoulos, Spyros Lalis, Nikolaos Bellas, Hans Vandierendonck, Dimitrios S. Nikolopoulos. **Exploiting Significance of Computa-**

tions for Energy-Constrained Approximate Computing. International Journal of Parallel Programming. 14 pages, 2016.

(A2) Articles not Included in the Science Citation Index, with Review Committee

1. Hans Vandierendonck and Koen De Bosschere. **An Address Transformation Combining Block- and Word-Interleaving**. Computer Architecture Letters, 1(2):14–17, July 2002
2. Lieven Eeckhout, Hans Vandierendonck and Koen De Bosschere. **Quantifying the Impact of Input Data Sets on Program Behavior and its Applications**. Journal of Instruction-Level Parallelism, 5:1-33, Februari 2003.
3. Veerle Desmet, Hans Vandierendonck and Koen De Bosschere. **2FAR: A 2bcgskew Predictor Fused by an Alloyed Redundant History Skewed Perceptron Branch Predictor**. Journal of Instruction-Level Parallelism (`http://www.jilp.org/`), 7:1-11, April 2005.
4. Hans Vandierendonck, Jean-Marie Jacquet, Bavo Nootaert and Koen De Bosschere. **Formaly Modeling Microprocessor Caches and Branch Predictors**. WSEAS Transactions on Computers, 5(11):2588-2595, 2006.
5. Hans Vandierendonck and André Seznec. **Fetch Gating Control through Speculative Instruction Window Weighting**. Transactions on High-Performance Embedded Achitectures and Compilation, 2(2):19–39, 2007.
6. Hans Vandierendonck and André Seznec. **Fairness Metrics for Multi-Threaded Processors**. IEEE Computer Architecture Letters, (RapidPosts), 4 pp., 2011.
7. Hans Vandierendonck, Ahmad Hassan and Dimitrios S. Nikolopoulos. **On the Energy-Efficiency of Byte-Addressable Non-Volatile Memory**. IEEE Computer Architecture Letters, (RapidPosts), 4 pp., 2015.

(A3) Articles not Included in the Science Citation Index, without Review Committee

1. Sean Rul, Hans Vandierendonck and Koen De Bosschere. **Function Level Parallelism Driven by Data Dependencies**. ACM SIGARCH Computer Architecture News, 35(1):55-62, 2007.

(C1) Articles in Proceedings of Scientific Conferences

1. Henk Neefs, Hans Vandierendonck and Koen De Bosschere. **A Technique for High Bandwidth and Deterministic Low Latency Load/Store Accesses to Multiple Cache Banks**. Proceedings of the 7th International Symposium on High Performance Computer Architecture, pp. 313–314, January 2000.
   Acceptance rate: 21%
2. Hans Vandierendonck and Koen De Bosschere. **A Comparison of Locality-Based and Recency-Based Replacement Policies**. Proceedings of the 3rd International Symposium on High-Performance Computing (ISHPC2k), pp. 310–318, October 2000.
3. Hans Vandierendonck and Koen De Bosschere. **An Optimal Replacement Policy for Balancing Multi-Module Caches**. Proceedings of the 12th Symposium on Computer Architecture and High Performance Computing, pp. 65–72, October 2000.
4. Bart Goeman, Hans Vandierendonck and Koen De Bosschere. **Differential FCM: Increasing Value Prediction Accuracy by Improving Table Usage Efficiency**. Proceedings of the 7th International Symposium on High Performance Computer Architecture, pp. 207–216, January 2001.
   Acceptance rate: 22%
5. Lieven Eeckhout, Tom Vander Aa, Bart Goeman, Hans Vandierendonck, Rudy Lauwereins and Koen De Bosschere. **Application Domains for Fixed-Length Block Structured Architectures**. Asia-Pacific Computer Systems Architecture Conference (ACSAC 2001), pages 35–44, January 2001.
6. Hans Vandierendonck and Koen De Bosschere. **Efficient Profile-Based Evaluation of Randomising Set Index Functions for Cache Memories**. 2nd International Symposium on Performance Analysis of Systems and Software, pages 120–127, November 2001.

7. Lieven Eeckhout, Hans Vandierendonck and Koen De Bosschere. **How Input Data Sets Change Program Behavior**, Workshop on Computer-Architecture Evaluation Using Commercial Workloads, in conjunction with HPCA-8, 9 pages, Februari 2002.
8. Tom Vander Aa, Lieven Eeckhout, Bart Goeman, Hans Vandierendonck, Rudy Lauwereins and Koen De Bosschere. **Optimizing a 3D Image Reconstruction Algorithm: Investigating the Interaction between the High-Level Implementation, the Compiler and the Architecture**. Asia-Pacific Computer Systems Architecture Conference (ACSAC 2002), pages 119–126, Februari 2002.
9. Hans Vandierendonck and Koen De Bosschere. **Evaluation of the Performance of Polynomial Set Index Functions**. Workshop on Duplicating, Deconstructing and Debunking, in conjunction with the 29th International Symposium on Computer Architecture, pages 31–41, May 2002.
10. Hans Vandierendonck, Alex Ramírez, Koen De Bosschere, and Mateo Valero. **A Comparative Study of Redundancy in Trace Caches**. Proceedings of the 8-th International Euro-Par Conference, pp. 512–516, August 2002.
11. Lieven Eeckhout, Hans Vandierendonck and Koen De Bosschere. **Workload Design: Selecting Representative Program-Input Pairs**. Proceedings of the 2002 International Conference on Parallel Architectures and Compilation Techniques, pp. 83-94, September 2002.
    Acceptance rate: 21%.
12. Hans Vandierendonck, Hans Logie and Koen De Bosschere. **Trace Substitution**. Proceedings of the 9-th International Euro-Par Conference, pp. 556–565, August 2003. Impact factor in 2002: 0,515.
13. Hans Vandierendonck and Koen De Bosschere. **Trade-Offs for Skewed-Associative Caches**. Proceedings of the International Conference ParCo2003, pages 467–474, September 2003
14. Hans Vandierendonck and Koen De Bosschere. **Many Benchmarks Stress the Same Bottlenecks**. Workshop on Computer-Architecture Evaluation Using Commercial Workloads, in conjunction with HPCA-10, pp. 57–64, Februari 2004.
15. Hans Vandierendonck and Koen De Bosschere. **Eccentric and Fragile Benchmarks**. 4th International Symposium on Performance Analysis of Systems and Software, pages 2–11, March 2004.
16. Hans Vandierendonck and Koen De Bosschere. **Experiments with Subsetting Benchmark Suites**. 7th Annual IEEE International Workshop on Workload Characterization, pages 55–62, October 2004.
17. Veerle Desmet, Hans Vandierendonck and Koen De Bosschere. **A 2bcgskew predictor fused by a redundant history skewed perceptron predictor**. 1st JILP Championship Branch Prediction. 4 pages, 2004.
    Branch prediction contest organized as a workshop. Finalist.
18. Pedro Trancoso, Christodoulos Adamou and Hans Vandierendonck. **Reducing TPC-H Benchmarking Time**. In Proceedings of the 10th Panhellenic Conference on Informatics (PCI 2005), 11 pages, November 2005.
19. Bavo Nootaert, Hans Vandierendonck and Koen De Bosschere. **Conflict Avoiding Caches Invite New Data Layout Optimizations**. The 10th Workshop on Interaction between Compilers and Computer Architectures (INTERACT). pages 23–33, Februari 2006.
20. Hans Vandierendonck, Philippe Manet and Jean-Didier Legat. **Application-Specific Reconfigurable XOR-Indexing to Eliminate Cache Conflict Misses**. Design Automation and Test Europe (DATE). pages 357–362, March 2006.
    Acceptance rate: 26%.
21. Joshua J. Yi, Hans Vandierendonck, Lieven Eeckhout and David J. Lilja. **The Exigency of Benchmark and Compiler Drift: Designing Tomorrow's Processor with Yesterday's Tools**. International Conference on Supercomputing. pages 75–86, July 2006.
    Acceptance rate: 26%.
22. Hans Vandierendonck and Pedro Trancoso. **Building and Validating a Reduced TPC-H Benchmark**. IEEE International Symposium on Modeling, Analysis, and Simulation of Computer and Telecommunica-

tion Systems (MASCOTS), pages 383–392, September 2006.

23. Hans Vandierendonck and Koen De Bosschere. **On the Impact of OS and Linker Effects on Level-2 Cache Performance**. IEEE International Symposium on Modeling, Analysis, and Simulation of Computer and Telecommunication Systems (MASCOTS). pages 87–95, September 2006.
24. Sean Rul, Hans Vandierendonck and Koen De Bosschere. **Function Level Parallelism Driven by Data Dependencies**. Workshop on Design, Architecture and Simulation of Chip Multi-Processors (dasCMP). 8 pages, December 2006.
25. Hans Vandierendonck and André Seznec. **Fetch Gating Control through Speculative Instruction Window Weighting**. 2nd International Conference on High-Performance Embedded Architectures and Compilation. pages 120–135, January 2007.
    Acceptance rate: 27%.
26. Hans Vandierendonck, Philippe Manet, Thibault Delavallée, Igor Loiselle, Jean-Didier Legat. **By-Passing the Out-of-Order Execution Pipeline to Increase Energy-Efficiency**. 4th International Conference on Computing Frontiers. pages 97–104, May 2007.
27. Hans Vandierendonck, Sean Rul, Michiel Questier, Koen De Bosschere. **Experiences with Parallelizing a Bio-Informatics Program on the Cell B.E.**. 3rd International Conference on High-Performance Embedded Architectures and Compilation. LNCS 4917, pages 161–175, January 2008.
    Acceptance rate: 29%.
28. Sean Rul, Hans Vandierendonck and Koen De Bosschere. **Detecting the Existence of Coarse-Grain Parallelism in General-Purpose Programs**. First Workshop on Programmability Issues for Multi-Core Computers (MULTIPROG-1). 12 pages, January 2008.
29. Hans Vandierendonck and Koen De Bosschere. **Constructing Optimal XOR-Functions to Minimize Cache Conflict Misses**. Achitecture of Computing Systems (ARCS). LNCS 4937, pages 261–272, March 2008.
30. Sean Rul, Hans Vandierendonck and Koen De Bosschere. **Extracting Coarse-Grain Parallelism in General-Purpose Programs**. ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming. pages 281–282, February 2008.
31. Sean Rul, Hans Vandierendonck and Koen De Bosschere. **Towards Automatic Program Partitioning**. 6th International Conference on Computing Frontiers. pages 89–98, May 2009.
32. Hans Vandierendonck, Sean Rul and Koen De Bosschere. **Factoring Out Ordered Sections to Increase Thread-Level Parallelism**. 2nd Workshop on Parallel Execution of Sequential Programs on Multicore Arhictectures, in conjunction with International Symposium on Computer Architecture. 8 pages, June 2009.
33. Sean Rul, Hans Vandierendonck and Koen De Bosschere. **Can We Apply Accelerator-Cores to Control Intensive Programs?** 2009 Symposium on Application Accelerators in High Performance Computing (SAAHPC'09). Organized by the National Center for Supercomputing Applications (NCSA), 3 pages, July 2009.
34. Sean Rul, Hans Vandierendonck, Joris D'Haene and Koen De Bosschere. **An Experimental Study on the Performance Portability of OpenCL Kernels**. 2010 Symposium on Application Accelerators in High Performance Computing (SAAHPC'10). Organized by the National Center for Supercomputing Applications (NCSA), 3 pages, July 2010.
35. Hans Vandierendonck, Sean Rul and Koen De Bosschere. **The Paralax Infrastructure: Automatic Parallelization with a Helping Hand**. 2010 IEEE International Conference on Parallel Architectures and Compilation Techniques. pp. 389–400, 2010.
    Acceptance rate: 17%
36. Hans Vandierendonck and Koen De Bosschere. **Implicit Hints: Embedding Hint Bits in Programs without ISA Changes**. 2010 IEEE International Conference on Computer Design. 6 pages, 2010.
37. Bertrand Rousseau, Philippe Manet, Igor Loiselle, Jean-Didier Legat and Hans Vandierendonck. **A Method-**

ology for Precise Comparisons of Processor Core Architectures for Homogeneous Many-Core DSP Platforms. Design and Architectures for Signal and Image Processing. 6 pages, 2010.

38. Hans Vandierendonck and Koen De Bosschere. **Whole-Array SSA: An Intermediate Representation of Memory for Trading-Off Precision against Complexity**. Workshop on Intermediate Representation. 8 pages, April 2011.
39. Hans Vandierendonck, Polyvios Pratikakis and Dimitrios S. Nikolopoulos. **Parallel Programming of General-Purpose Programs Using Task-Based Programming Models**. 3rd USENIX Workshop on Hot Topics in Parallelism. 6 pages, 2011.
40. Thibault Delavallée, Philippe Manet, Jean-Didier Legat and Hans Vandierendonck. **Application-based workload model for wireless sensor node computing platforms**. 10th Faible Tension Faible Consommation. June 2011.
41. Thibault Delavallée, Philippe Manet, Jean-Didier Legat and Hans Vandierendonck. **Embedding functional simulators in compilers for debugging and profiling**. 10th Faible Tension Faible Consommation. June 2011.
42. Polyvios Pratikakis, Hans Vandierendonck, Spyros Lyberis and Dimitrios S. Nikolopoulos. **A programming model for deterministic task parallelism**. In: 6th Workshop on Memory Systems Performance and Correctness. In conjunction with International Symposium on Programming Language Design and Implementation (PLDI). June 2011.
43. Hans Vandierendonck and Koen De Bosschere. **Automatic Parallelization in the Paralax Compiler**. Workshop on Software and Compilers for Embedded Systems (SCOPES). **Invited paper**. 8 pages, June 2011.
44. Hans Vandierendonck, George Tzenakis and Dimitrios S. Nikolopoulos. **A Unified Scheduler for Recursive and Task-Based Parallelism**. 2011 IEEE International Conference on Parallel Architectures and Compilation Techniques. Accepted for publication, 2011. *Acceptance rate: 16%*
45. George Tzenakis, Angelos Papatriantafyllou, John Kesapides, Polyvios Pratikakis, Hans Vandierendonck and Dimitrios S. Nikolopoulos. **BDDT: Block-Level Dynamic Dependence Analysis for Deterministic Task-Based Parallelism**. 17th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming. pp. 301–302, 2012.
46. George Tzenakis, Angelos Papatriantafyllou, Polyvios Pratikakis, Hans Vandierendonck and Dimitrios S. Nikolopoulos. **BDDT: Block-Level Dynamic Dependence Analysis for Deterministic Task-Based Parallelism (full version)**. 10th International Symposium on Advanced Parallel Processing Technologies. pp. 17–31, 2013.
47. Hans Vandierendonck, Kallia Chronaki, Dimitrios S. Nikolopoulos. **Deterministic Scale-Free Pipeline Parallelism with Hyperqueues.** SC '13 Proceedings of the International Conference on High Performance Computing, Networking, Storage and Analysis. 12 pages, 2013.
48. Konstantin Bakanov, Ivor Spence, Hans Vandierendonck and Charles Gillan. **Rigorous Specification and Low-Latency Implementation of Technical Market Indicators.** Workshop on Parallel Programming for Analytics Applications, 9 pages, 2014.
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